B.E

Information Science and Engineering

VISVESVARAYA TECHNOLOGICAL

UNIVERSITY, BELGAUM

ENGINEERING MATHEMATICS – III

CODE: 10 MAT 31	**IA Marks: 25**
Hrs/Week: 04	**Exam Hrs: 03**
Total Hrs: 52	**Exam**
Marks:100	

PART-A

Unit-I: FOURIER SERIES

Convergence and divergence of infinite series of positive terms, definition and illustrative examples*
Periodic functions, Dirichlet's conditions, Fourier series of periodic functions of period 2π and arbitrary period, half range Fourier series. Complex form of Fourier Series. Practical harmonic analysis. **[7 hours]**

Unit-II: FOURIER TRANSFORMS

Infinite Fourier transform, Fourier Sine and Cosine transforms, properties, Inverse transforms
[6 hours]

Unit-III: APPLICATIONS OF PDE

Various possible solutions of one dimensional wave and heat equations, two dimensional Laplace's equation by the method of separation of variables, Solution of all these equations with specified boundary conditions. D'Alembert's solution of one dimensional wave equation.
[6 hours]

Unit-IV: CURVE FITTING AND OPTIMIZATION

Curve fitting by the method of least squares- Fitting of curves of the form $y = ax+b,\quad y=a\,x^2 + b\,x+c,$ $y = a\,e^{bx}$, $y = ax^b$

Optimization: Linear programming, mathematical formulation of linear programming problem (LPP), Graphical method and simplex method.

[7 hours]

PART-B

Unit-V: NUMERICAL METHODS - 1

Numerical Solution of algebraic and transcendental equations: Regula-falsi method, Newton - Raphson method. Iterative methods of solution of a system of equations: Gauss-seidel and Relaxation methods. Largest eigen value and the corresponding eigen vector by Rayleigh's power method.

[6 hours]

Unit-VI: NUMERICAL METHODS – 2

Finite differences: Forward and backward differences, Newton's forward and backward interpolation formulae. Divided differences - Newton's divided difference formula, Lagrange's interpolation formula and inverse interpolation formula.

Numerical integration: Simpson's one-third, three-eighth and Weddle's rules (All formulae/rules without proof)

[7 hours]

Unit-VII: NUMERICAL METHODS – 3

Numerical solutions of PDE – finite difference approximation to derivatives, Numerical solution of two dimensional Laplace's equation, one dimensional heat and wave equations

[7 hours]

<u>Unit-VIII:</u> DIFFERENCE EQUATIONS AND Z-TRANSFORMS

Difference equations: Basic definition; Z-transforms – definition, standard Z-transforms, damping rule, shifting rule, initial value and final value theorems. Inverse Z-transform. Application of Z-transforms to solve difference equations.

[6 hours]

Note: * In the case of illustrative examples, questions are not to be set.

<u>Text Books:</u>

1. B.S. Grewal, Higher Engineering Mathematics, Latest edition, Khanna Publishers
2. Erwin Kreyszig, Advanced Engineering Mathematics, Latest edition, Wiley Publications.

<u>Reference Book:</u>

1. B.V. Ramana, Higher Engineering Mathematics, Latest edition, Tata Mc. Graw Hill Publications.
2. Peter V. O’Neil, Engineering Mathematics, CENGAGE Learning India Pvt Ltd.Publishers

ELECTRONIC CIRCUITS
(Common to CSE & ISE)

Subject Code: 10CS32	**I.A. Marks : 25**
Hours/Week : 04	**Exam Hours: 03**

Total Hours : 52 **Exam Marks: 100**

PART - A

UNIT - 1 **7 Hours**

Transistors, UJTs, and Thyristors: Operating Point, Common-Emitter Configuration, Thermal Runaway, Transistor Switch, Unijunction Transistors, SCR.

UNIT - 2 **6 Hours**

Field Effect Transistors: Bipolar Junction Transistors versus Field Effect Transistors, Junction Field Effect Transistors, Metal Oxide Field Effect Transistors, Differences between JFETs and MOSFETs, Handling MOSFETs, Biasing MOSFETs, FET Applications, CMOS Devices, Insulated Gate Bipolar Transistors (IGBTs)

UNIT - 3 **6 Hours**

Optoelectronic Devices: Introduction, Photosensors, Photoconductors, Photodiodes, Phototransistors, Light-Emitting Diodes, Liquid Crystal Displays, Cathode Ray Tube Displays, Emerging Display Technologies, Optocouplers

UNIT - 4 **7 Hours**

Small Signal Analysis of Amplifiers: Amplifier Bandwidth: General Frequency Considerations, Hybrid h-Parameter Model for an Amplifier, Transistor Hybrid Model, Analysis of a Transistor Amplifier using complete h-Parameter Model, Analysis of a Transistor Amplifier Configurations using Simplified h-Parameter Model (CE configuration only), Small-Signal Analysis of FET Amplifiers, Cascading Amplifiers, Darlington Amplifier, Low-Frequency Response of Amplifiers (BJT amplifiers only).

PART - B

UNIT - 5 **6 Hours**

Large Signal Amplifiers, Feedback Amplifier: Classification and characteristics of Large Signal Amplifiers, Feedback Amplifiers: Classification of Amplifiers, Amplifier with Negative Feedback, Advantages of Negative Feedback, Feedback Topologies, Voltage-Series (Series-Shunt) Feedback, Voltage-Shunt (Shunt-Shunt) Feedback, Current-Series (Series-Series) Feedback, Current-Shunt (Shunt-Series) Feedback.

UNIT - 6 **7 Hours**

Sinusoidal Oscillators, Wave-Shaping Circuits: Classification of Oscillators, Conditions for Oscillations: Barkhausen Criterion, Types of Oscillators, Crystal Oscillator, Voltage-Controlled Oscillators, Frequency Stability.

Wave-Shaping Circuits: Basic RC Low-Pass Circuit, RC Low-Pass Circuit as Integrator, Basic RC High-Pass Circuit, RC High-Pass Circuit as Differentiator, Multivibrators, Integrated Circuit (IC) Multivibrators.

UNIT - 7 7 Hours

Linear Power Supplies, Switched mode Power Supplies: Linear Power Supplies: Constituents of a Linear Power Supply, Designing Mains Transformer; Linear IC Voltage Regulators, Regulated Power Supply Parameters.

Switched Mode Power Supplies: Switched Mode Power Supplies, Switching Regulators, Connecting Power Converters in Series, Connecting Power Converters in Parallel.

UNIT - 8 6 Hours

Operational Amplifiers: Ideal Opamp versus Practical Opamp, Performance Parameters, Some Applications: Peak Detector Circuit, Absolute Value Circuit, Comparator, Active Filters, Phase Shifters, Instrumentation Amplifier, Non-Linear Amplifier, Relaxation Oscillator, Current-To-Voltage Converter, Voltage-To-Current Converter, Sine Wave Oscillators.

Text Book:

1. Anil K Maini, Varsha Agarwal: Electronic Devices and Circuits, Wiley, 2009.

(4.1, 4.2, 4.7, 4.8, 5.1 to 5.3, 5.5, 5.6, 5.8, 5.9, 5.13, 5.14, 6.1, 6.3, 7.1 to 7.5, 7.10 to 7.14, Listed topics only from 8, 10.1, 11, 12.1, 12.2, 12.3, 12.5, 13.1 to 13.6, 13.9, 13.10, 14.1, 14.2, 14.6, 14.7, 15.1, 15.5 to 15.7. 16.3, 16.4, 17.12 to 17.22)

Reference Books:

1. Jacob Millman, Christos Halkias, Chetan D Parikh: Millman's Integrated Electronics – Analog and Digital Circuits and Systems, 2nd Edition, Tata McGraw Hill, 2010.
2. R. D. Sudhaker Samuel: Electronic Circuits, Sanguine-Pearson, 2010.

LOGIC DESIGN
(Common to CSE & ISE)

Subject Code: 10CS33	**I.A. Marks : 25**
Hours/Week : 04	**Exam Hours: 03**
Total Hours : 52	**Exam Marks: 100**

PART-A

UNIT – 1 **7 Hours**

Digital Principles, Digital Logic: Definitions for Digital Signals, Digital Waveforms, Digital Logic, 7400 TTL Series, TTL Parameters The Basic Gates: NOT, OR, AND, Universal Logic Gates: NOR, NAND, Positive and Negative Logic, Introduction to HDL.

UNIT – 2 **6 Hours**

Combinational Logic Circuits

Sum-of-Products Method, Truth Table to Karnaugh Map, Pairs Quads, and Octets, Karnaugh Simplifications, Don't-care Conditions, Product-of-sums Method, Product-of-sums simplifications, Simplification by Quine-McClusky Method, Hazards and Hazard Covers, HDL Implementation Models.

UNIT – 3 **6 Hours**

Data-Processing Circuits: Multiplexers, Demultiplexers, 1-of-16 Decoder, Encoders, Exclusive-or Gates, Parity Generators and Checkers, Magnitude Comparator, Programmable Array Logic, Programmable Logic Arrays, HDL Implementation of Data Processing Circuits

UNIT – 4 **7 Hours**

Clocks, Flip-Flops: Clock Waveforms, TTL Clock, Schmitt Trigger, Clocked D FLIP-FLOP, Edge-triggered D FLIP-FLOP, Edge-triggered JK FLIP-FLOP, FLIP-FLOP Timing, JK Master-slave FLIP-FLOP, Switch Contact Bounce Circuits, Various Representation of FLIP-FLOPs, Analysis of Sequential Circuits, HDL Implementation of FLIP-FLOP

PART-B

UNIT – 5 **6 Hours**

Registers: Types of Registers, Serial In - Serial Out, Serial In - Parallel out, Parallel In - Serial Out, Parallel In - Parallel Out, Universal Shift Register, Applications of Shift Registers, Register Implementation in HDL

UNIT – 6 **7 Hours**

Counters: Asynchronous Counters, Decoding Gates, Synchronous Counters, Changing the Counter Modulus, Decade Counters, Presettable Counters, Counter Design as a Synthesis problem, A Digital Clock, Counter Design using HDL

UNIT – 7 **7 Hours**

Design of Synchronous and Asynchronous Sequential Circuits: Design of Synchronous Sequential Circuit: Model Selection, State Transition Diagram, State Synthesis Table, Design Equations and Circuit Diagram, Implementation using Read Only Memory, Algorithmic State Machine, State Reduction Technique.

Asynchronous Sequential Circuit: Analysis of Asynchronous Sequential Circuit, Problems with Asynchronous Sequential Circuits, Design of Asynchronous Sequential Circuit, FSM Implementation in HDL

UNIT – 8 6 Hours

D/A Conversion and A/D Conversion: Variable, Resistor Networks, Binary Ladders, D/A Converters, D/A Accuracy and Resolution, A/D Converter-Simultaneous Conversion, A/D Converter-Counter Method, Continuous A/D Conversion, A/D Techniques, Dual-slope A/D Conversion, A/D Accuracy and Resolution

Text Book:

1. Donald P Leach, Albert Paul Malvino & Goutam Saha: Digital Principles and Applications, 7th Edition, Tata McGraw Hill, 2010.

Reference Books:

1. Stephen Brown, Zvonko Vranesic: Fundamentals of Digital Logic Design with VHDL, 2nd Edition, Tata McGraw Hill, 2005.
2. R D Sudhaker Samuel: Illustrative Approach to Logic Design, Sanguine-Pearson, 2010.
3. Charles H. Roth: Fundamentals of Logic Design, Jr., 5th Edition, Cengage Learning, 2004.
4. Ronald J. Tocci, Neal S. Widmer, Gregory L. Moss: Digital Systems Principles and Applications, 10th Edition, Pearson Education, 2007.
5. M Morris Mano: Digital Logic and Computer Design, 10th Edition, Pearson Education, 2008.

DISCRETE MATHEMATICAL STRUCTURES
(Common to CSE & ISE)

Subject Code: 10CS34	**I.A. Marks : 25**
Hours/Week : 04	**Exam Hours: 03**
Total Hours : 52	**Exam Marks: 100**

PART – A

UNIT – 1 **6 Hours**

Set Theory: Sets and Subsets, Set Operations and the Laws of Set Theory, Counting and Venn Diagrams, A First Word on Probability, Countable and Uncountable Sets

UNIT – 2 **7 Hours**

Fundamentals of Logic: Basic Connectives and Truth Tables, Logic Equivalence – The Laws of Logic, Logical Implication – Rules of Inference

UNIT – 3 **6 Hours**

Fundamentals of Logic *contd.*: The Use of Quantifiers, Quantifiers, Definitions and the Proofs of Theorems

UNIT – 4 **7 Hours**

Properties of the Integers: Mathematical Induction, The Well Ordering Principle – Mathematical Induction, Recursive Definitions

PART – B

UNIT – 5 **7 Hours**

Relations and Functions: Cartesian Products and Relations, Functions – Plain and One-to-One, Onto Functions – Stirling Numbers of the Second Kind, Special Functions, The Pigeon-hole Principle, Function Composition and Inverse Functions

UNIT – 6 **7 Hours**

Relations *contd.*: Properties of Relations, Computer Recognition – Zero-One Matrices and Directed Graphs, Partial Orders – Hasse Diagrams, Equivalence Relations and Partitions

UNIT – 7 **6 Hours**

Groups: Definitions, Examples, and Elementary Properties, Homomorphisms, Isomorphisms, and Cyclic Groups, Cosets, and Lagrange’s Theorem.

Coding Theory and Rings: Elements of Coding Theory, The Hamming Metric, The Parity Check, and Generator Matrices

UNIT – 8 **6 Hours**

Group Codes: Decoding with Coset Leaders, Hamming Matrices
Rings and Modular Arithmetic: The Ring Structure – Definition and Examples, Ring Properties and Substructures, The Integers Modulo n

Text Book:

1. Ralph P. Grimaldi: Discrete and Combinatorial Mathematics, , 5th Edition, Pearson Education, 2004.
   (Chapter 3.1, 3.2, 3.3, 3.4, Appendix 3, Chapter 2, Chapter 4.1, 4.2, Chapter 5.1 to 5.6, Chapter 7.1 to 7.4, Chapter 16.1, 16.2, 16.3, 16.5 to 16.9, and Chapter 14.1, 14.2, 14.3).

Reference Books:

1. Kenneth H. Rosen: Discrete Mathematics and its Applications, 7th Edition, McGraw Hill, 2010.
2. Jayant Ganguly: A Treatise on Discrete Mathematical Structures, Sanguine-Pearson, 2010.
3. D.S. Malik and M.K. Sen: Discrete Mathematical Structures: Theory and Applications, Cengage Learning, 2004.
4. Thomas Koshy: Discrete Mathematics with Applications, Elsevier, 2005, Reprint 2008.

DATA STRUCTURES WITH C
(Common to CSE & ISE)

Subject Code: 10CS35	**I.A. Marks : 25**
Hours/Week : 04	**Exam Hours: 03**
Total Hours : 52	**Exam Marks: 100**

PART – A

UNIT - 1 **8 Hours**

BASIC CONCEPTS: Pointers and Dynamic Memory Allocation, Algorithm Specification, Data Abstraction, Performance Analysis, Performance Measurement

UNIT -2 **6 Hours**

ARRAYS and STRUCTURES: Arrays, Dynamically Allocated Arrays, Structures and Unions, Polynomials, Sparse Matrices, Representation of Multidimensional Arrays

UNIT - 3 **6 Hours**

STACKS AND QUEUES: Stacks, Stacks Using Dynamic Arrays, Queues, Circular Queues Using Dynamic Arrays, Evaluation of Expressions, Multiple Stacks and Queues.

UNIT - 4 **6 Hours**

LINKED LISTS: Singly Linked lists and Chains, Representing Chains in C, Linked Stacks and Queues, Polynomials, Additional List operations, Sparse Matrices, Doubly Linked Lists

PART - B

UNIT - 5 **6 Hours**

TREES – 1: Introduction, Binary Trees, Binary Tree Traversals, Threaded Binary Trees, Heaps.

UNIT – 6 **6 Hours**

TREES – 2, GRAPHS: Binary Search Trees, Selection Trees, Forests, Representation of Disjoint Sets, Counting Binary Trees, The Graph Abstract Data Type.

UNIT - 7 **6 Hours**

PRIORITY QUEUES Single- and Double-Ended Priority Queues, Leftist Trees, Binomial Heaps, Fibonacci Heaps, Pairing Heaps.

UNIT - 8 **8 Hours**

EFFICIENT BINARY SEARCH TREES: Optimal Binary Search Trees, AVL Trees, Red-Black Trees, Splay Trees.

Text Book:

1. Horowitz, Sahni, Anderson-Freed: Fundamentals of Data Structures in C, 2nd Edition, Universities Press, 2007.
   (Chapters 1, 2.1 to 2.6, 3, 4, 5.1 to 5.3, 5.5 to 5.11, 6.1, 9.1 to 9.5, 10)

Reference Books:

1. Yedidyah, Augenstein, Tannenbaum: Data Structures Using C and C++, 2nd Edition, Pearson Education, 2003.
2. Debasis Samanta: Classic Data Structures, 2nd Edition, PHI, 2009.
3. Richard F. Gilberg and Behrouz A. Forouzan: Data Structures A Pseudocode Approach with C, Cengage Learning, 2005.
4. Robert Kruse & Bruce Leung: Data Structures & Program Design in C, Pearson Education, 2007.

OBJECT ORIENTED PROGRAMMING WITH C++
(Common to CSE & ISE)

Subject Code: 10CS36	**I.A. Marks : 25**
Hours/Week : 04	**Exam Hours: 03**
Total Hours : 52	**Exam Marks: 100**

PART – A

UNIT 1 6 Hours

Introduction: Overview of C++, Sample C++ program, Different data types, operators, expressions, and statements, arrays and strings, pointers & user-defined types

Function Components, argument passing, inline functions, function overloading, recursive functions

UNIT 2 7 Hours

Classes & Objects – I: Class Specification, Class Objects, Scope resolution operator, Access members, Defining member functions, Data hiding, Constructors, Destructors, Parameterized constructors, Static data members, Functions

UNIT 3 7 Hours

Classes & Objects –II: Friend functions, Passing objects as arguments, Returning objects, Arrays of objects, Dynamic objects, Pointers to objects, Copy constructors, Generic functions and classes, Applications

Operator overloading using friend functions such as +, - , pre-increment, post-increment, [ ] etc., overloading <<, >>.

UNIT 4 6 Hours

Inheritance – I: Base Class, Inheritance and protected members, Protected base class inheritance, Inheriting multiple base classes

PART – B

UNIT 5 6 Hours

Inheritance – II: Constructors, Destructors and Inheritance, Passing parameters to base class constructors, Granting access, Virtual base classes

UNIT 6 7 Hours

Virtual functions, Polymorphism: Virtual function, Calling a Virtual function through a base class reference, Virtual attribute is inherited, Virtual functions are hierarchical, Pure virtual functions, Abstract classes, Using virtual functions, Early and late binding.

UNIT 7 **6 Hours**

I/O System Basics, File I/0: C++ stream classes, Formatted I/O, I/O manipulators, fstream and the File classes, File operations

UNIT 8 **7 Hours**

Exception Handling, STL: Exception handling fundamentals, Exception handling options

STL: An overview, containers, vectors, lists, maps.

Text Books:

1. Herbert Schildt: The Complete Reference C++, 4th Edition, Tata McGraw Hill, 2003.

Reference Books:

1. Stanley B.Lippmann, Josee Lajore: C++ Primer, 4th Edition, Pearson Education, 2005.
2. Paul J Deitel, Harvey M Deitel: C++ for Programmers, Pearson Education, 2009.
3. K R Venugopal, Rajkumar Buyya, T Ravi Shankar: Mastering C++, Tata McGraw Hill, 1999.

DATA STRUCTURES WITH C/C++ LABORATORY
(Common to CSE & ISE)

Subject Code: 10CSL37	**I.A. Marks : 25**
Hours/Week : 03	**Exam Hours: 03**
Total Hours : 42	**Exam Marks: 50**

1. Using circular representation for a polynomial, design, develop, and execute a program in C to accept two polynomials, add them, and then print the resulting polynomial.

2. Design, develop, and execute a program in C to convert a given valid parenthesized infix arithmetic expression to postfix expression and then to print both the expressions. The expression consists of single character operands and the binary operators + (plus), - (minus), * (multiply) and / (divide).

3. Design, develop, and execute a program in C to evaluate a valid postfix expression using stack. Assume that the postfix expression is read as a single line consisting of non-negative single digit operands

and binary arithmetic operators. The arithmetic operators are + (add), - (subtract), * (multiply) and / (divide).

4. Design, develop, and execute a program in C to simulate the working of a queue of integers using an array. Provide the following operations:
a. Insert b. Delete c. Display

5. Design, develop, and execute a program in C++ based on the following requirements:
An EMPLOYEE class is to contain the following data members and member functions:
Data members: Employee_Number (an integer), Employee_Name (a string of characters), Basic_Salary (an integer) , All_Allowances (an integer), IT (an integer), Net_Salary (an integer).
Member functions: to read the data of an employee, to calculate Net_Salary and to print the values of all the data members.
(All_Allowances = 123% of Basic; Income Tax (IT) = 30% of the gross salary (= basic_Salary _ All_Allowance); Net_Salary = Basic_Salary + All_Allowances – IT)

6. Design, develop, and execute a program in C++ to create a class called STRING and implement the following operations. Display the results after every operation by overloading the operator <<.
   i. STRING s1 = “VTU”
   ii. STRING s2 = “BELGAUM”
   iii. STIRNG s3 = s1 + s2; (Use copy constructor)

7. Design, develop, and execute a program in C++ to create a class called STACK using an array of integers and to implement the following operations by overloading the operators + and - :
   i. s1=s1 + element; where s1 is an object of the class STACK and element is an integer to be pushed on to top of the stack.
   ii. s1=s1- ; where s1 is an object of the class STACK and – operator pops off the top element.

   Handle the STACK Empty and STACK Full conditions. Also display the contents of the stack after each operation, by overloading the operator <<.

8. Design, develop, and execute a program in C++ to create a class called LIST (linked list) with member functions to insert an element at the front of the list as well as to delete an element from the front of the list. Demonstrate all the functions after creating a list object.

9. Design, develop, and execute a program in C to read a sparse matrix of integer values and to search the sparse matrix for an element specified by the user. Print the result of the search appropriately. Use the triple <row, column, value> to represent an element in the sparse matrix.

10. Design, develop, and execute a program in C to create a max heap of integers by accepting one element at a time and by inserting it immediately in to the heap. Use the array representation for the heap. Display the array at the end of insertion phase.

11. Design, develop, and execute a program in C to implement a doubly linked list where each node consists of integers. The program should support the following operations:
    i. Create a doubly linked list by adding each node at the front.
    ii. Insert a new node to the left of the node whose key value is read as an input.
    iii. Delete the node of a given data if it is found, otherwise display appropriate message.
    iv. Display the contents of the list.

(Note: Only either (a,b and d) or (a, c and d) may be asked in the examination)

12. Design, develop, and execute a program in C++ to create a class called DATE with methods to accept two valid dates in the form dd/mm/yy and to implement the following operations by overloading the operators + and -. After every operation the results are to be displayed by overloading the operator <<.
    i. no_of_days = d1 – d2; where d1 and d2 are DATE objects, d1 >=d2 and no_of_days is an integer.
    ii. d2 = d1 + no_of_days; where d1 is a DATE object and no_of_days is an integer.

13. Design, develop, and execute a program in C++ to create a class called OCTAL, which has the characteristics of an octal number. Implement the following operations by writing an appropriate constructor and an overloaded operator +.
    i. OCTAL h = x ; where x is an integer
    ii. int y = h + k ; where h is an OCTAL object and k is an integer.

    Display the OCTAL result by overloading the operator <<. Also display the values of h and y.

14. Design, develop, and execute a program in C++ to create a class called BIN_TREE that represents a Binary Tree, with member functions to perform inorder, preorder and postorder traversals. Create a BIN_TREE object and demonstrate the traversals.

Note: In the examination each student picks one question from a lot of *all* the 14 questions.

ELECTRONIC CIRCUITS & LOGIC DESIGN LABORATORY
(Common to CSE & ISE)

Subject Code: 10CSL38	**I.A. Marks : 25**
Hours/Week : 03	**Exam Hours: 03**
Total Hours : 42	**Exam Marks : 50**

PART-A

1. a) Design and construct a suitable circuit and demonstrate the working of positive clipper, double-ended clipper and positive clamper using diodes.
   b) Demonstrate the working of the above circuits using a simulation package.

2. a) Design and construct a suitable circuit and determine the frequency response, input impedance, output impedance, and bandwidth of a CE amplifier.
   b) Design and build the CE amplifier circuit using a simulation package and determine the voltage gain for two different values of supply voltage and for two different values of emitter resistance.

3. a) Design and construct a suitable circuit and determine the drain characteristics and transconductance characteristics of an enhancement-mode MOSFET.
   b) Design and build CMOS inverter using a simulation package and verify its truth table.

4. a) Design and construct a Schmitt trigger using Op-Amp for given UTP and LTP values and demonstrate its working.
   b) Design and implement a Schmitt trigger using Op-Amp using a simulation package for two sets of UTP and LTP values and demonstrate its working.

5. a) Design and construct a rectangular waveform generator (Op-Amp relaxation oscillator) for given frequency and demonstrate its working.
   b) Design and implement a rectangular waveform generator (Op-Amp relaxation oscillator) using a simulation package and demonstrate the change in frequency when all resistor values are doubled.

6. Design and implement an astable multivibrator circuit using 555 timer for a given frequency and duty cycle.

PART – B

7. a) Given a 4-variable logic expression, simplify it using Entered Variable Map and realize the simplified logic expression using 8:1 multiplexer IC.
   b) Design and develop the Verilog /VHDL code for an 8:1 multiplexer. Simulate and verify its working.

8. a) Realize a J-K Master / Slave Flip-Flop using NAND gates and verify its truth table.
   b) Design and develop the Verilog / VHDL code for D Flip-Flop with positive-edge triggering. Simulate and verify its working.

9. a) Design and implement a mod-n (n<8) synchronous up counter using J-K Flip-Flop ICs and demonstrate its working.
   b) Design and develop the Verilog / VHDL code for mod-8 up counter. Simulate and verify its working.

10. a) Design and implement a ring counter using 4-bit shift register and demonstrate its working.
    b) Design and develop the Verilog / VHDL code for switched tail counter. Simulate and verify its working.

11. Design and implement an asynchronous counter using decade counter IC to count up from 0 to n (n<=9) and demonstrate its working.

12. Design and construct a 4-bit R-2R ladder D/A converter using Op-Amp. Determine its accuracy and resolution.

Notes:

1. **In the examination, each student picks one question from the lot of questions, either from Part-A or from Part-B. About half the students in the batch are to get a question from Part-A while the rest are to get the question from Part-B.**
2. **Any simulation package like MultiSim / Pspice etc may be used.**

IV SEMESTER

ENGINEERING MATHEMATICS – IV

CODE: 10 MAT 41	**IA Marks: 25**
Hrs/Week: 04	**Exam Hrs: 03**
Total Hrs: 52	**Exam**
Marks:100	

PART-A

Unit-I: NUMERICAL METHODS - 1

Numerical solution of ordinary differential equations of first order and first degree; Picard’s method, Taylor’s series method, modified Euler’s method, Runge-kutta method of fourth-order. Milne’s and Adams - Bashforth predictor and corrector methods (No derivations of formulae).

[6 hours]

Unit-II: NUMERICAL METHODS – 2

Numerical solution of simultaneous first order ordinary differential equations: Picard’s method, Runge-Kutta method of fourth-order.

Numerical solution of second order ordinary differential equations: Picard's method, Runge-Kutta method and Milne's method.

[6 hours]

Unit-III: Complex variables – 1

Function of a complex variable, Analytic functions-Cauchy-Riemann equations in cartesian and polar forms. Properties of analytic functions.
Application to flow problems- complex potential, velocity potential, equipotential lines, stream functions, stream lines.

[7 hours]

Unit-IV: Complex variables – 2

Conformal Transformations: Bilinear Transformations. Discussion of Transformations: $w = z^2$, $\mathrm{w} = e^z$, $w = z + (a^2 / z)$. Complex line integrals-Cauchy's theorem and Cauchy's integral formula.

[7 hours]

PART-B

Unit-V: SPECIAL FUNCTIONS

Solution of Laplace equation in cylindrical and spherical systems leading Bessel's and Legendre's differential equations, Series solution of Bessel's differential equation leading to Bessel function of first kind. Orthogonal property of Bessel functions. Series solution of Legendre's differential equation leading to Legendre polynomials, Rodrigue's formula.

[7 hours]

Unit-VI: PROBABILITY THEORY - 1

Probability of an event, empherical and axiomatic definition, probability associated with set theory, addition law, conditional probability, multiplication law, Baye's theorem.

[6 hours]

Unit-VII: PROBABILITY THEORY- 2

Random variables (discrete and continuous), probability density function, cumulative density function. Probability distributions – Binomial and Poisson distributions; Exponential and normal distributions.

[7 hours]

Unit-VIII: SAMPLING THEORY

Sampling, Sampling distributions, standard error, test of hypothesis for means, confidence limits for means, student's t-distribution. Chi -Square distribution as a test of goodness of fit

[6 hours]

Text Books:

1. B.S. Grewal, Higher Engineering Mathematics, Latest edition, Khanna Publishers
2. Erwin Kreyszig, Advanced Engineering Mathematics, Latest edition, Wiley Publications.

Reference Book:

1. B.V. Ramana, Higher Engineering Mathematics, Latest edition, Tata Mc. Graw Hill Publications.
2. Peter V. O'Neil, Engineering Mathematics, CENGAGE Learning India Pvt Ltd.Publishers

GRAPH THEORY AND COMBINATORICS
(Common to CSE & ISE)

Subject Code: 10CS42	**I.A. Marks : 25**
Hours/Week : 04	**Exam Hours: 03**
Total Hours : 52	**Exam Marks: 100**

PART – A

UNIT - 7 Hours

Introduction to Graph Theory: Definitions and Examples, Subgraphs, Complements, and Graph Isomorphism, Vertex Degree, Euler Trails and Circuits

UNIT - 2 6 Hours

Introduction to Graph Theory *contd.*: Planar Graphs, Hamilton Paths and Cycles, Graph Colouring, and Chromatic Polynomials

UNIT - 3 6 Hours

Trees: Definitions, Properties, and Examples, Routed Trees, Trees and Sorting, Weighted Trees and Prefix Codes

UNIT - 4 7 Hours

Optimization and Matching: Dijkstra's Shortest Path Algorithm, Minimal Spanning Trees – The algorithms of Kruskal and Prim, Transport Networks – Max-flow, Min-cut Theorem, Matching Theory

PART – B

UNIT - 5 **6 Hours**

Fundamental Principles of Counting: The Rules of Sum and Product, Permutations, Combinations – The Binomial Theorem, Combinations with Repetition, The Catalon Numbers

UNIT - 6 **6 Hours**

The Principle of Inclusion and Exclusion: The Principle of Inclusion and Exclusion, Generalizations of the Principle, Derangements – Nothing is in its Right Place, Rook Polynomials

UNIT - 7 **7 Hours**

Generating Functions: Introductory Examples, Definition and Examples – Calculational Techniques, Partitions of Integers, the Exponential Generating Function, the Summation Operator

UNIT - 8 **7 Hours**

Recurrence Relations: First Order Linear Recurrence Relation, The Second Order Linear Homogeneous Recurrence Relation with Constant Coefficients, The Non-homogeneous Recurrence Relation, The Method of Generating Functions

Text Book:

1. Ralph P. Grimaldi: Discrete and Combinatorial Mathematics, 5th Edition, Pearson Education, 2004.
   (Chapter 11, Chapter 12.1 to 12.4, Chapter 13, Chapter 1, Chapter 8.1 to 8.4, Chapter 9 Chapter 10.1 to 10.4).

Reference Books:

1. D.S. Chandrasekharaiah: Graph Theory and Combinatorics, Prism, 2005.
2. Chartrand Zhang: Introduction to Graph Theory, TMH, 2006.
3. Richard A. Brualdi: Introductory Combinatorics, 4th Edition, Pearson Education, 2004.
4. Geir Agnarsson & Raymond Geenlaw: Graph Theory, Pearson Education, 2007.

DESIGN AND ANALYSIS OF ALGORITHMS
(Common to CSE & ISE)

Subject Code: 10CS43	**I.A. Marks : 25**
Hours/Week : 04	**Exam Hours: 03**

Total Hours : 52 **Exam Marks: 100**

PART – A

UNIT – 1 **7 Hours**

INTRODUCTION: Notion of Algorithm, Review of Asymptotic Notations, Mathematical Analysis of Non-Recursive and Recursive Algorithms
Brute Force Approaches: Introduction, Selection Sort and Bubble Sort, Sequential Search and Brute Force String Matching.

UNIT - 2 **6 Hours**

DIVIDE AND CONQUER: Divide and Conquer: General Method, Defective Chess Board, Binary Search, Merge Sort, Quick Sort and its performance.

UNIT - 3 **7 Hours**

THE GREEDY METHOD: The General Method, Knapsack Problem, Job Sequencing with Deadlines, Minimum-Cost Spanning Trees: Prim's Algorithm, Kruskal's Algorithm; Single Source Shortest Paths.

UNIT - 4 **6 Hours**

DYNAMIC PROGRAMMING: The General Method, Warshall's Algorithm, Floyd's Algorithm for the All-Pairs Shortest Paths Problem, Single-Source Shortest Paths: General Weights, 0/1 Knapsack, The Traveling Salesperson problem.

PART – B

UNIT - 5 **7 Hours**

DECREASE-AND-CONQUER APPROACHES, SPACE-TIME TRADEOFFS: Decrease-and-Conquer Approaches: Introduction, Insertion Sort, Depth First Search and Breadth First Search, Topological Sorting
Space-Time Tradeoffs: Introduction, Sorting by Counting, Input Enhancement in String Matching.

UNIT – 6 **7 Hours**

LIMITATIONS OF ALGORITHMIC POWER AND COPING WITH THEM: Lower-Bound Arguments, Decision Trees, P, NP, and NP-Complete Problems, Challenges of Numerical Algorithms.

UNIT - 7 **6 Hours**

COPING WITH LIMITATIONS OF ALGORITHMIC POWER: Backtracking: n - Queens problem, Hamiltonian Circuit Problem, Subset – Sum Problem.

Branch-and-Bound: Assignment Problem, Knapsack Problem, Traveling Salesperson Problem.
Approximation Algorithms for NP-Hard Problems – Traveling Salesperson Problem, Knapsack Problem

UNIT – 8 **6 Hours**
PRAM ALGORITHMS: Introduction, Computational Model, Parallel Algorithms for Prefix Computation, List Ranking, and Graph Problems,

Text Books:

1. Anany Levitin: Introduction to The Design & Analysis of Algorithms, 2nd Edition, Pearson Education, 2007.
   (Listed topics only from the Chapters 1, 2, 3, 5, 7, 8, 10, 11).
2. Ellis Horowitz, Sartaj Sahni, Sanguthevar Rajasekaran: Fundamentals of Computer Algorithms, 2nd Edition, Universities Press, 2007.
   (Listed topics only from the Chapters 3, 4, 5, 13)

Reference Books:

1. Thomas H. Cormen, Charles E. Leiserson, Ronal L. Rivest, Clifford Stein: Introduction to Algorithms, 3rd Edition, PHI, 2010.
2. R.C.T. Lee, S.S. Tseng, R.C. Chang & Y.T.Tsai: Introduction to the Design and Analysis of Algorithms A Strategic Approach, Tata McGraw Hill, 2005.

UNIX AND SHELL PROGRAMMING
(Common to CSE & ISE)

Subject Code: 10CS44	**I.A. Marks : 25**
Hours/Week : 04	**Exam Hours: 03**
Total Hours : 52	**Exam Marks: 100**

PART – A

UNIT – 1 **6 Hours**
The Unix Operating System, The UNIX architecture and Command Usage, The File System

UNIT - 2 **6 Hours**
Basic File Attributes, the vi Editor

UNIT - 3 **7 Hours**
The Shell, The Process, Customizing the environment

UNIT - 4 **7 Hours**

More file attributes, Simple filters

PART – B

UNIT - 5 **6 Hours**

Filters using regular expressions,

UNIT - 6 **6 Hours**

Essential Shell Programming

UNIT - 7 **7 Hours**

awk – An Advanced Filter

UNIT - 8 **7 Hours**

perl - The Master Manipulator

Text Book:

1. Sumitabha Das: UNIX – Concepts and Applications, 4th Edition, Tata McGraw Hill, 2006.
   (Chapters 1.2, 2, 4, 6, 7, 8, 9, 10, 11, 12, 13, 14, 18, 19)

Reference Books:

1. Behrouz A. Forouzan and Richard F. Gilberg: UNIX and Shell Programming**,** Cengage Learning, 2005.
2. M.G. Venkateshmurthy: UNIX & Shell Programming**,** Pearson Education, 2005.

MICROPROCESSORS
(Common to CSE & ISE)

Subject Code: 10CS45	**I.A. Marks : 25**
Hours/Week : 04	**Exam Hours: 03**
Total Hours : 52	**Exam Marks: 100**

PART A

UNIT – 1 **7 Hours**

Introduction, Microprocessor Architecture – 1: A Historical Background, The Microprocessor-Based Personal Computer Systems.

The Microprocessor and its Architecture: Internal Microprocessor Architecture, Real Mode Memory Addressing.

UNIT – 2 7 Hours

Microprocessor Architecture – 2, Addressing Modes: Introduction to Protected Mode Memory Addressing, Memory Paging, Flat Mode Memory
Addressing Modes: Data Addressing Modes, Program Memory Addressing Modes, Stack Memory Addressing Modes

UNIT – 3 6 Hours

Programming – 1: Data Movement Instructions: MOV Revisited, PUSH/POP, Load-Effective Address, String Data Transfers, Miscellaneous Data Transfer Instructions, Segment Override Prefix, Assembler Details.
Arithmetic and Logic Instructions: Addition, Subtraction and Comparison, Multiplication and Division.

UNIT - 4 6 Hours

Programming – 2: Arithmetic and Logic Instructions (continued): BCD and ASCII Arithmetic, Basic Logic Instructions, Shift and Rotate, String Comparisons.
Program Control Instructions: The Jump Group, Controlling the Flow of the Program, Procedures, Introduction to Interrupts, Machine Control and Miscellaneous Instructions.

PART B

UNIT - 5 6 Hours

Programming – 3: Combining Assembly Language with C/C++: Using Assembly Language with C/C++ for 16-Bit DOS Applications and 32-Bit Applications
Modular Programming, Using the Keyboard and Video Display, Data Conversions, Example Programs

UNIT - 6 7 Hours

Hardware Specifications, Memory Interface – 1: Pin-Outs and the Pin Functions, Clock Generator, Bus Buffering and Latching, Bus Timings, Ready and Wait State, Minimum versus Maximum Mode.
Memory Interfacing: Memory Devices

UNIT – 7 6 Hours

Memory Interface – 2, I/O Interface – 1: Memory Interfacing (continued): Address Decoding, 8088 Memory Interface, 8086 Memory Interface.
Basic I/O Interface: Introduction to I/O Interface, I/O Port Address Decoding.

UNIT 8 7 Hours

I/O Interface – 2, Interrupts, and DMA: I/O Interface (continued): The Programmable Peripheral Interface 82C55, Programmable Interval Timer 8254.
Interrupts: Basic Interrupt Processing, Hardware Interrupts: INTR and INTA/; Direct Memory Access: Basic DMA Operation and Definition.

Text Book:

1. Barry B Brey: The Intel Microprocessors, 8th Edition, Pearson Education, 2009.
   (Listed topics only from the Chapters 1 to 13)

Reference Books:

1. Douglas V. Hall: Microprocessors and Interfacing, Revised 2nd Edition, TMH, 2006.
2. K. Udaya Kumar & B.S. Umashankar : Advanced Microprocessors & IBM-PC Assembly Language Programming, TMH 2003.
3. James L. Antonakos: The Intel Microprocessor Family: Hardware and Software Principles and Applications, Cengage Learning, 2007.

COMPUTER ORGANIZATION
(Common to CSE & ISE)

Subject Code: 10CS46	**I.A. Marks : 25**
Hours/Week : 04	**Exam Hours: 03**
Total Hours : 52	**Exam Marks: 100**

PART – A

UNIT - 1 6 Hours

Basic Structure of Computers: Computer Types, Functional Units, Basic Operational Concepts, Bus Structures, Performance – Processor Clock, Basic Performance Equation, Clock Rate, Performance Measurement, Historical Perspective
Machine Instructions and Programs: Numbers, Arithmetic Operations and Characters, Memory Location and Addresses, Memory Operations, Instructions and Instruction Sequencing,

UNIT - 2 7 Hours

Machine Instructions and Programs *contd*.: Addressing Modes, Assembly Language, Basic Input and Output Operations, Stacks and Queues, Subroutines, Additional Instructions, Encoding of Machine Instructions

UNIT - 3 6 Hours

Input/Output Organization: Accessing I/O Devices, Interrupts – Interrupt Hardware, Enabling and Disabling Interrupts, Handling Multiple Devices, Controlling Device Requests, Exceptions, Direct Memory Access, Buses

UNIT - 4 **7 Hours**

Input/Output Organization ***contd*****.:** Interface Circuits, Standard I/O Interfaces – PCI Bus, SCSI Bus, USB

PART – B

UNIT - 5 **7 Hours**

Memory System: Basic Concepts, Semiconductor RAM Memories, Read Only Memories, Speed, Size, and Cost, Cache Memories – Mapping Functions, Replacement Algorithms, Performance Considerations, Virtual Memories, Secondary Storage

UNIT - 6 **7 Hours**

Arithmetic: Addition and Subtraction of Signed Numbers, Design of Fast Adders, Multiplication of Positive Numbers, Signed Operand Multiplication, Fast Multiplication, Integer Division, Floating-point Numbers and Operations

UNIT - 7 **6 Hours**

Basic Processing Unit: Some Fundamental Concepts, Execution of a Complete Instruction, Multiple Bus Organization, Hard-wired Control, Microprogrammed Control

UNIT - 8 **6 Hours**

Multicores, Multiprocessors, and Clusters: Performance, The Power Wall, The Switch from Uniprocessors to Multiprocessors, Amdahl's Law, Shared Memory Multiprocessors, Clusters and other Message Passing Multiprocessors, Hardware Multithreading, SISD, IMD, SIMD, SPMD, and Vector.

Text Books:

1. Carl Hamacher, Zvonko Vranesic, Safwat Zaky: Computer Organization, 5th Edition, Tata McGraw Hill, 2002.
   (Listed topics only from Chapters 1, 2, 4, 5, 6, 7)
2. David A. Patterson, John L. Hennessy: Computer Organization and Design – The Hardware / Software Interface ARM Edition, 4th Edition, Elsevier, 2009.
3. (Listed topics only)

Reference Books:

1. William Stallings: Computer Organization & Architecture, 7th Edition, PHI, 2006.

2. Vincent P. Heuring & Harry F. Jordan: Computer Systems Design and Architecture, 2nd Edition, Pearson Education, 2004.

DESIGN AND ANALYSIS OF ALGORITHMS LABORATORY
(Common to CSE & ISE)

Subject Code: 10CSL47	**I.A. Marks : 25**
Hours/Week : 03	**Exam Hours: 03**
Total Hours : 42	**Exam Marks: 50**

Design, develop and implement the specified algorithms for the following problems using C/C++ Language in LINUX / Windows environment.

1. Sort a given set of elements using the Quicksort method and determine the time required to sort the elements. Repeat the experiment for different values of n, the number of elements in the list to be sorted and plot a graph of the time taken versus n.
   The elements can be read from a file or can be generated using the random number generator.

2. Using OpenMP, implement a parallelized Merge Sort algorithm to sort a given set of elements and determine the time required to sort the elements. Repeat the experiment for different values of n, the number of elements in the list to be sorted and plot a graph of the time taken versus n. The elements can be read from a file or can be generated using the random number generator.

3. a. Obtain the Topological ordering of vertices in a given digraph.
   b. Compute the transitive closure of a given directed graph using Warshall's algorithm.

4. Implement 0/1 Knapsack problem using Dynamic Programming.

5. From a given vertex in a weighted connected graph, find shortest paths to other vertices using Dijkstra's algorithm.

6. Find Minimum Cost Spanning Tree of a given undirected graph using Kruskal's algorithm.

7. a. Print all the nodes reachable from a given starting node in a digraph using BFS method.
   b. Check whether a given graph is connected or not using DFS method.

8. Find a subset of a given set S = {sl,s2,.....,sn} of n positive integers whose sum is equal to a given positive integer d. For example, if S= {1, 2, 5, 6, 8} and d = 9 there are two solutions{1,2,6}and{1,8}.A suitable message is to be displayed if the given problem instance doesn't have a solution.

9. Implement any scheme to find the optimal solution for the Traveling Salesperson problem and then solve the same problem instance using any approximation algorithm and determine the error in the approximation.

10. Find Minimum Cost Spanning Tree of a given undirected graph using Prim’s algorithm.

11. Implement All-Pairs Shortest Paths Problem using Floyd's algorithm. Parallelize this algorithm, implement it using OpenMP and determine the speed-up achieved.

12. Implement N Queen's problem using Back Tracking.

Note: In the examination *each* student picks one question from the lot of *all* 12 questions.

MICROPROCESSORS LABORATORY
(Common to CSE & ISE)

Subject Code : 10CSL48	**I.A. Marks : 25**
Hours/Week : 03	**Exam Hours: 03**
Total Hours : 42	**Exam Marks: 50**

Notes:

- **Develop and execute the following programs using 8086 Assembly Language. Any suitable assembler like MASM, TASM etc may be used.**
- **Program should have suitable comments.**

- **The board layout and the circuit diagram of the interface are to be provided to the student during the examination.**

1. a) Search a key element in a list of ‘n’ 16-bit numbers using the Binary search algorithm.

   b) Read the status of eight input bits from the Logic Controller Interface and display ‘FF’ if it is the parity of the input read is even; otherwise display 00.

2. a) Write two ALP modules stored in two different files; one module is to read a character from the keyboard and the other one is to display a character. Use the above two modules to read a string of characters from the keyboard terminated by the carriage return and print the string on the display in the next line.

   b) Implement a BCD Up-Down Counter on the Logic Controller Interface.

3. a) Sort a given set of ‘n’ numbers in ascending order using the Bubble Sort algorithm.

   b) Read the status of two 8-bit inputs (X & Y) from the Logic Controller Interface and display X*Y.

4. a) Read an alphanumeric character and display its equivalent ASCII code at the center of the screen.

   b) Display messages FIRE and HELP alternately with flickering effects on a 7-segment display interface for a suitable period of time. Ensure a flashing rate that makes it easy to read both the messages (Examiner does not specify these delay values nor is it necessary for the student to compute these values).

5. a) Reverse a given string and check whether it is a palindrome or not.

   b) Assume any suitable message of 12 characters length and display it in the rolling fashion on a 7-segment display interface for a suitable period of time. Ensure a flashing rate that makes it easy to read both the messages. (Examiner does not specify these delay values nor is it necessary for the student to compute these values).

6. a) Read two strings, store them in locations STR1 and STR2. Check whether they are equal or not and display appropriate messages. Also display the length of the stored strings.

b) Convert a 16-bit binary value (assumed to be an unsigned integer) to BCD and display it from left to right and right to left for specified number of times on a 7-segment display interface.

7. a) Read your name from the keyboard and display it at a specified location on the screen after the message "**What is your name?"** You must clear the entire screen before display.

   b) Scan a 8 x 3 keypad for key closure and to store the code of the key pressed in a memory location or display on screen. Also display row and column numbers of the key pressed.

8. a) Compute **nCr** using recursive procedure. Assume that 'n' and 'r' are non-negative integers.

   b) Drive a Stepper Motor interface to rotate the motor in specified direction (clockwise or counter-clockwise) by N steps (Direction and N are specified by the examiner). Introduce suitable delay between successive steps. (Any arbitrary value for the delay may be assumed by the student).

9. a) Read the current time from the system and display it in the standard format on the screen.

   b) Generate the Sine Wave using DAC interface (The output of the DAC is to be displayed on the CRO).

10. a) Write a program to simulate a Decimal Up-counter to display 00-99.

    b) Generate a Half Rectified Sine wave form using the DAC interface. (The output of the DAC is to be displayed on the CRO).

11. a) Read a pair of input co-ordinates in BCD and move the cursor to the specified location on the screen.

    b) Generate a Fully Rectified Sine waveform using the DAC interface. (The output of the DAC is to be displayed on the CRO).

12. a) Write a program to create a file (input file) and to delete an existing file.

    b) Drive an elevator interface in the following way:

       i. Initially the elevator should be in the ground floor, with all requests in OFF state.

       ii. When a request is made from a floor, the elevator should move to that floor, wait there for a couple of seconds (approximately), and then come down to ground floor and